ABSTRACT OF THE DISCLOSURE

An n-bit shift register 102 for shifting input data through successive bit stages and AND gates 103-i (i being 1 to n) corresponding to the bit stages of the shift register 102 are provided. A control circuit 101 feeds out control signals 107-i for on-off controlling the feeding of the outputs of the corresponding bit stages of the shift register 102. Multipliers 104-i multiply the on-off controlled data and predetermined filter coefficient data, and an adder circuit 105 adds together the output of the multipliers to derive an FIR filter output including ramp-up and -down. A ramp-up/-down signal is fed to a shift register in the control circuit 101, and ramp-up data is derived from the output of the adder circuit 105. Thus, the circuit can be readily constructed without scale increase.